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DATA SHEET

TEA1207UK
High efficiency DC/DC converter Chip Scale package

Product specification

2002 Jul 03

Philips Semiconductors

PHILIPS

High efficiency DC/DC converter Chip Scale package

TEA1207UK

FEATURES

- Fully integrated DC/DC converter circuit
- Up-or-down conversion
- Start-up from 1.85 V input voltage
- Adjustable output voltage
- High efficiency over large load range
- Power handling capability up to 0.85 A continuous average current
- 275 kHz switching frequency
- Low quiescent power consumption
- Synchronizing with external clock
- True current limit for Li-ion battery compatibility
- Up to 100% duty cycle in down mode
- Undervoltage lockout
- Shut-down function
- 2×2 mm footprint chip scale package.

APPLICATIONS

- Cellular and cordless phones, Personal Digital Assistants (PDAs) and others
- Supply voltage source for low-voltage chip sets
- Portable computers
- Battery backup supplies
- Cameras.

GENERAL DESCRIPTION

The TEA1207UK is a fully integrated DC/DC converter. Efficient, compact and dynamic power conversion is achieved using a novel digitally controlled concept such as Pulse Width Modulation (PWM) or Pulse Frequency Modulation (PFM), integrated low R_{DSon} CMOS power switches with low parasitic capacitances, and fully synchronous rectification.

The device operates at a 275 kHz switching frequency which enables the use of external components with minimum size. Deadlock is prevented by an on-chip undervoltage lockout circuit.

Efficient behaviour during short load peaks and compatibility with Li-ion batteries is guaranteed by an accurate current limiting function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1207UK	LFBGA8	plastic low profile fine-pitch ball grid array package; 8 balls; body $2 \times 2 \times 0.46$ mm	–

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
UPCONVERSION; BALL $\overline{U}$/D = LOW						
V_I	input voltage		$V_{I(start)}$	–	5.50	V
V_O	output voltage		2.80	–	5.50	V
$V_{I(start)}$	start-up input voltage	I_L < 125 mA	1.40	1.60	1.85	V
DOWNCONVERSION; BALL $\overline{U}$/D = HIGH						
V_I	input voltage		2.80	–	5.50	V
V_O	output voltage		1.30	–	5.50	V
GENERAL						
V_{fb}	feedback voltage		1.19	1.24	1.29	V
Current levels						
I_q	quiescent current on ball A1	down mode; V_I = 3.6 V	52	65	72	µA
I_{shdwn}	current in shut-down state		–	2	10	µA
I_{LX}	maximum continuous current on ball A2	T_{amb} = 60 °C	–	–	0.85	A
ΔI_{lim}	current limiting deviation	I_{lim} = 0.5 to 5 A				
		up mode	–17.5	–	+17.5	%
		down mode	–17.5	–	+17.5	%
Power MOSFETs						
R_{DSon}	drain-to-source on-state resistance					
	N-type		0.10	0.20	0.30	Ω
	P-type		0.10	0.22	0.35	Ω
Efficiency						
η1	efficiency upconversion	V_I = 3.6 V; V_O = 4.6 V; L1 = 10 µH				
		I_L = 1 mA	–	88	–	%
		I_L = 200 mA	–	95	–	%
		I_L = 1 A; pulsed	–	83	–	%
η2	efficiency downconversion	V_I = 3.6 V; V_O = 2.0 V; L1 = 10 µH				
		I_L = 1 mA	–	86	–	%
		I_L = 200 mA	–	93	–	%
		I_L = 1 A; pulsed	–	81	–	%
Timing						
f_{sw}	switching frequency	PWM mode	220	275	330	kHz
f_{sync}	synchronization clock input frequency		4	6.5	20	MHz
t_{res}	response time	from standby to $P_{o(max)}$	–	50	–	µs

BLOCK DIAGRAM

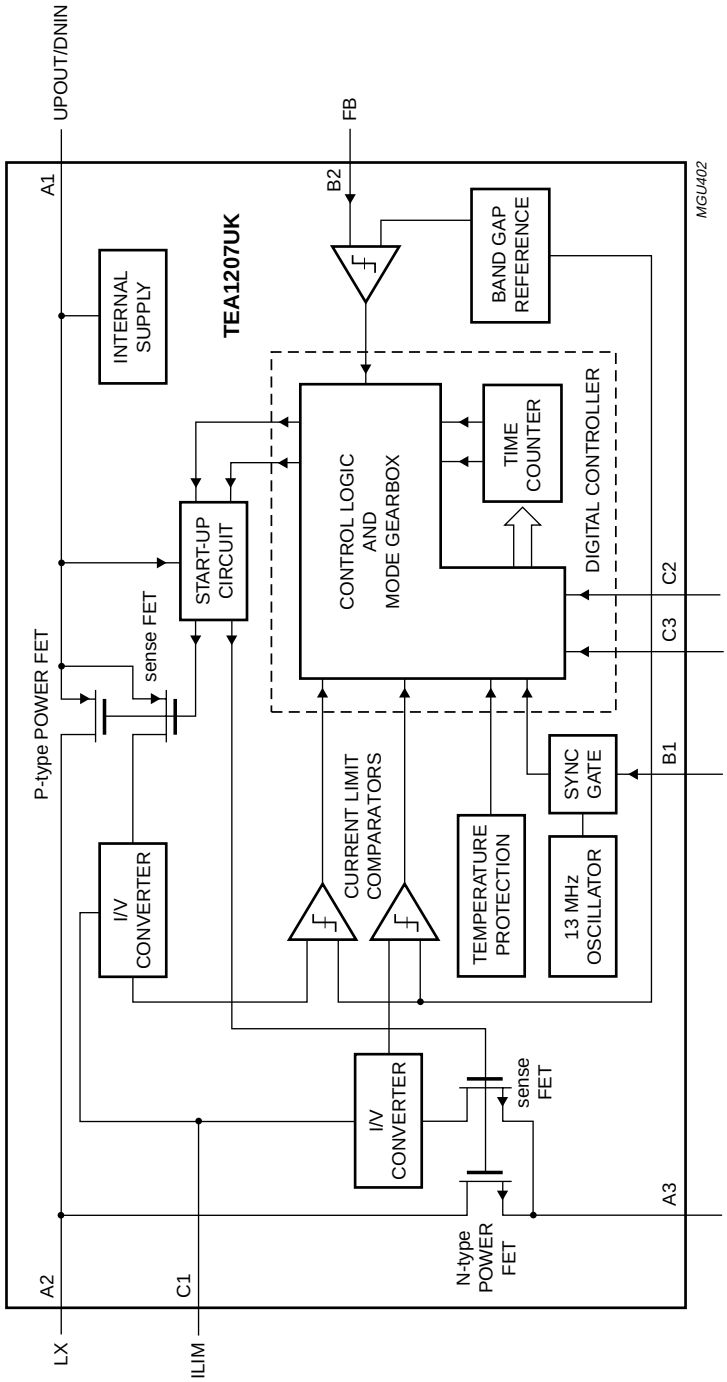


Fig.1 Block diagram.

PINNING

SYMBOL	BALL	DESCRIPTION
UPOUT/DNIN	A1	output voltage in up mode; input voltage in down mode
LX	A2	inductor connection
GND	A3	ground
SYNC	B1	synchronization clock input
FB	B2	feedback input
ILIM	C1	current limiting resistor connection
$\overline{U}$/D	C2	up-or-down mode selection input; active LOW for up mode
SHDWN	C3	shut-down input

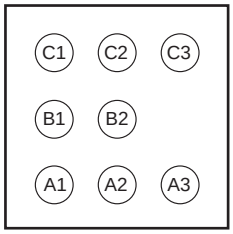


Fig.2 Ball configuration (bottom view).

FUNCTIONAL DESCRIPTION

Control mechanism

The TEA1207UK is able to operate in PFM (discontinuous conduction) or PWM (continuous conduction) operating mode. All switching actions are completely determined by a digital control circuit which uses the output voltage level as its control input. This novel digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete operating range of the converter.

When high output power is requested, the device will operate in the PWM mode. This results in minimum AC currents in the circuit components and hence optimum efficiency, minimum cost and low EMC. In this operating mode, the output voltage is allowed to vary between two predefined voltage levels. As long as the output voltage stays within this so-called window, switching continues in a fixed pattern. When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the pulse width and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations. Figure 3 shows the converter's response to a sudden load increase. The upper trace shows the output voltage. The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, times the capacitor's internal Equivalent Series Resistance (ESR). After each ramp-down of the inductor current, i.e. when the ESR effect increases the output voltage, the converter determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay.

When the output voltage becomes lower than the low limit of the window, a corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue. The output voltage (including ESR effect) is again within the predefined window. Figure 4 shows the spread of the output voltage window. The absolute value is most dependent on spread, while the actual window size is not affected. For one specific device, the output voltage will not vary more than 2% typical.

In low output power situations, the TEA1207UK will switch over to PFM mode. In this mode, regulation information from earlier PWM operating modes is used. This results in optimum inductor peak current levels in the PFM mode, which are slightly larger than the inductor ripple current in the PWM mode. As a result, the transition between PFM and PWM mode is optimum under all circumstances. In the PFM mode the TEA1207UK regulates the output voltage to the high window limit shown in Fig.3.

Synchronous rectification

For optimum efficiency over the whole load range, synchronous rectifiers within the TEA1207UK ensure that during the whole second switching phase, all inductor current will flow through the low-ohmic power MOSFETs. Special circuitry is included which detects when the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds with regulation.

Start-up

Start-up from low input voltage in boost mode is realized by an independent start-up oscillator, which starts switching the N-type power MOSFET as soon as the voltage at ball UPOUT/DNIN is sufficiently high. The switch actions of the start-up oscillator will increase the output voltage. As soon as the output voltage is high enough for normal regulation, the digital control system takes over the control of the power MOSFETs.

Undervoltage lockout

As a result of too high load or disconnection of the input power source, the output voltage can drop so low that normal regulation cannot be guaranteed. In this event, the device switches back to start-up mode. If the output voltage drops down even further, switching is stopped completely.

Shut-down

When the shut-down input is made HIGH, the converter disables both power switches and the power consumption is reduced to a few microamperes.

Power switches

The power switches in the IC are one N-type and one P-type power MOSFET, having a typical drain-to-source resistance of 0.20 and 0.22 Ω respectively. The maximum average current in the power switches is 0.60 A at T_{amb} = 80 °C.

Temperature protection

When the device operates in the PWM mode, and the die temperature gets too high (typically 175 °C), the converter stops operating. It resumes operation when the die temperature falls below 175 °C again. As a result, low frequent cycling between the on and off state will occur. It should be noted that in the event of a device temperature around the cut-off limit, the application will differ strongly from the maximum specification.

Current limiters

If the current in one of the power switches exceeds its limit in the PWM mode, the current ramp is stopped immediately, and the next switching phase is entered. Current limiting is required to enable optimum use of energy in Li-ion batteries, and to keep power conversion efficient during temporary high loads. Furthermore, current limiting protects the IC against overload conditions, inductor saturation, etc. The current limiting level is set by an external resistor.

External synchronization

If an external high frequency clock is applied to the synchronization clock input, the switching frequency in PWM mode will be exactly that frequency divided by 22. In PFM mode, the switching frequency is always lower. The quiescent current of the device increases when external clock pulses are applied. If no external synchronization is necessary, the synchronization clock input must be connected to ground.

Behaviour when the input voltage exceeds the specified range

In general, an input voltage exceeding the specified range is not recommended since instability may occur. There are two exceptions:

- Upconversion: at an input voltage higher than the target output voltage, but up to 6 V, the converter will stop switching and the internal P-type power MOSFET will be conducting. The output voltage will equal the input voltage minus some resistive voltage drop. The current limiting function is not active.
- Downconversion: when the input voltage is lower than the target output voltage, but higher than 2.8 V, the P-type power MOSFET will stay conducting resulting in an output voltage being equal to the input voltage minus some resistive voltage drop. The current limiting function remains active.

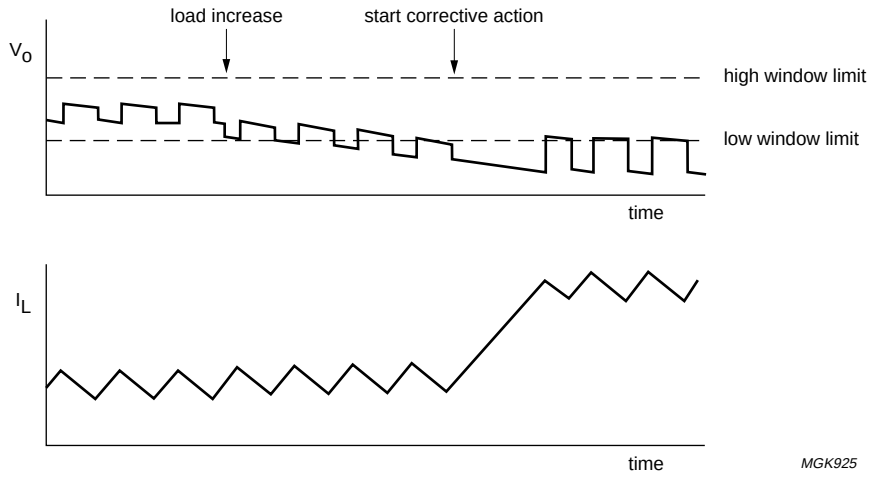


Fig.3 Response to load increase.

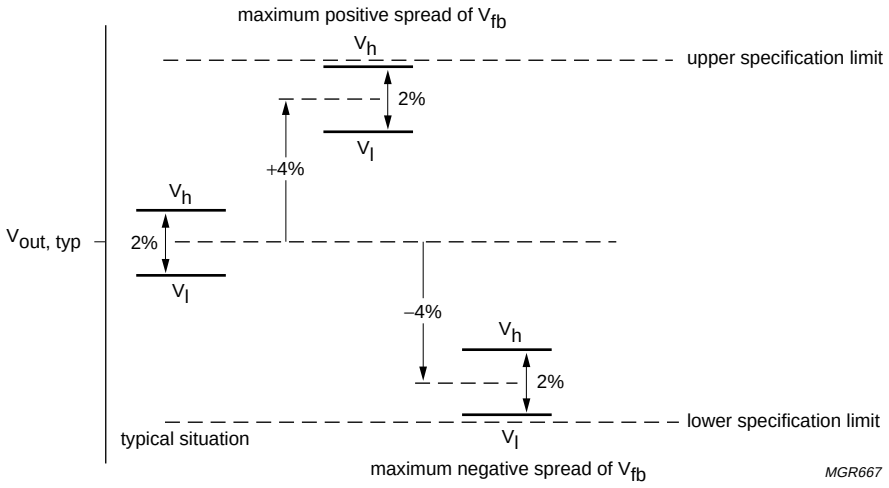


Fig.4 Spread of location of output voltage window.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any ball	shut-down mode	−0.2	+6.5	V
		operating mode	−0.2	+5.9	V
T_j	junction temperature		−25	+150	°C
T_{amb}	ambient temperature		−40	+80	°C
T_{stg}	storage temperature		−40	+125	°C
V_{es}	electrostatic handling voltage	human body model; note 1	−4000	+4000	V
		machine model; note 2	−300	+300	V

Notes

1. Class 3; equivalent to discharging a 100 pF capacitor through a 1500 resistor.
2. Class 2; equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to Printed-Circuit Board (PCB)	in free air; note 1	145	K/W

Note

1. The thermal resistance is highly dependent on printed-circuit board type and metal routing. The value given is valid for a single metal layer printed-circuit board.

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611 part E”*.

CHARACTERISTICS

T_{amb} = –40 to +80 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
UPCONVERSION; BALL $\overline{U}$/D = LOW						
V_i	input voltage		$V_{I(start)}$	–	5.50	V
V_o	output voltage		2.80	–	5.50	V
$V_{i(start)}$	start-up input voltage	I_L < 125 mA	1.40	1.60	1.85	V
$V_{i(uvlo)}$	undervoltage lockout input voltage	note 1	1.50	2.10	2.50	V
DOWNCONVERSION; BALL $\overline{U}$/D = HIGH						
V_i	input voltage	note 2	2.80	–	5.50	V
V_o	output voltage		1.30	–	5.50	V
GENERAL						
V_{fb}	feedback input voltage		1.19	1.24	1.29	V
ΔV_{wdw}	output voltage window	PWM mode	1.5	2.0	3.0	%
Current levels						
I_q	quiescent current on ball A1	down mode; V_3 = 3.0 V; note 3	52	65	72	µA
I_{shdwn}	current in shut-down mode		–	2	10	µA
I_{LX}	maximum continuous current on ball A2	T_{amb} = 60 °C	–	–	0.85	A
		T_{amb} = 80 °C	–	–	0.60	A
ΔI_{lim}	current limit deviation	I_{lim} = 0.5 to 5.0 A; note 4				
		up mode	–17.5	–	+17.5	%
		down mode	–17.5	–	+17.5	%
Power MOSFETs						
R_{DSon}	drain-to-source on-state resistance					
	N-type		0.10	0.20	0.30	Ω
	P-type		0.10	0.22	0.35	Ω
Efficiency						
η1	efficiency upconversion	V_I = 3.6 V; V_O = 4.6 V; L1 = 10 µH; note 5				
		I_L = 1 mA	–	88	–	%
		I_L = 10 mA	–	93	–	%
		I_L = 50 mA	–	93	–	%
		I_L = 100 mA	–	94	–	%
		I_L = 200 mA	–	95	–	%
		I_L = 500 mA	–	92	–	%
		I_L = 1 A; pulsed	–	83	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\eta 2$	efficiency downconversion	V_I = 3.6 V; V_O = 2.0 V; L1 = 10 µH; note 5				
		I_L = 1 mA	–	86	–	%
		I_L = 10 mA	–	91	–	%
		I_L = 50 mA	–	92	–	%
		I_L = 100 mA	–	92	–	%
		I_L = 200 mA	–	93	–	%
		I_L = 500 mA	–	89	–	%
		I_L = 1 A; pulsed	–	81	–	%
Timing						
f_{sw}	switching frequency	PWM mode	220	275	330	kHz
f_{sync}	synchronization clock input frequency		4	6.5	20	MHz
t_{res}	response time	from standby to $P_{o(max)}$	–	50	–	µs
Temperature						
T_{amb}	ambient temperature		–40	+25	+80	°C
$T_{co(max)}$	maximum internal cut-off temperature		150	175	200	°C
Digital levels						
V_{IL}	LOW-level input voltage on balls B1, C2 and C3		0	–	0.4	V
V_{IH}	HIGH-level input voltage	note 6				
	on ball C2		V_3 – 0.4	–	V_3 + 0.3	V
	on balls B1 and C3		$0.55V_3$	–	V_3 + 0.3	V

Notes

1. The undervoltage lockout voltage shows wide specification limits since it decreases at increasing temperature. When the temperature increases, the minimum supply voltage of the digital control part of the IC decreases and therefore the correct operation of this function is guaranteed over the whole temperature range.
2. When V_i is lower than the target output voltage but higher than 2.8 V, the P-type power MOSFET will remain conducting (100% duty cycle), resulting in V_o following V_i.
3. V_3 is the voltage on ball A1 (UPOUT/DNIN).
4. The current limit is defined by the external resistor R_{lim} (see Section “Current limiting resistors”). Accuracy of the current limit increases in proportion to the programmed current limiting level.
5. The specified efficiency is valid when using an output capacitor having an ESR of 0.10 Ω and a 10 µH small size inductor (Coilcraft DT1608C-103).
6. If the applied HIGH-level voltage is less than V_3 to 1 V, the quiescent current (I_q) of the device will increase.

APPLICATION INFORMATION

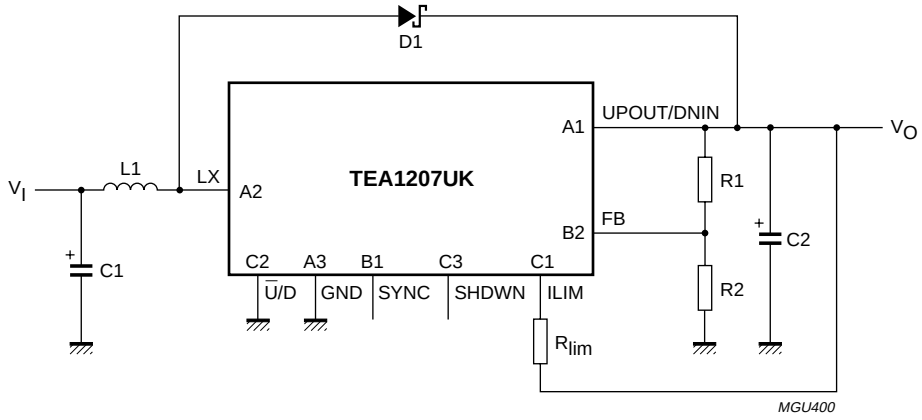


Fig.5 Complete application diagram for upconversion.

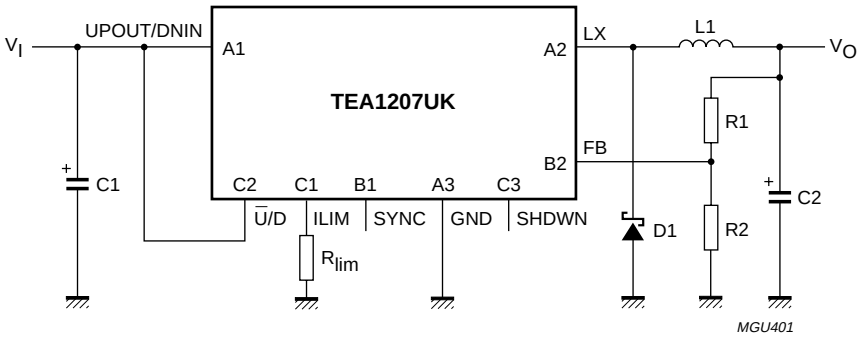


Fig.6 Complete application diagram for downconversion.

External component selection

INDUCTOR L1

The performance of the TEA1207UK is not very sensitive to inductance value. Best efficiency performance over a wide load current range is achieved by using e.g. TDK SLF7032-6R8M1R6, having an inductance of 6.8 μH and a saturation current level of 1.6 A. In case the maximum output current is lower, other inductors are also suitable such as the small sized Coilcraft DT1608 range.

INPUT CAPACITOR C1

The value of capacitor C1 strongly depends on the type of input source. In general, a 100 μF tantalum capacitor will do, or a 10 μF ceramic capacitor featuring very low series resistance (ESR value).

OUTPUT CAPACITOR C2

The value and type of capacitor C2 depend on the maximum output current and the ripple voltage which is allowed in the application. Low-ESR tantalum capacitors show good results. The most important specification of capacitor C2 is its ESR, which mainly determines the output voltage ripple.

DIODE D1

The Schottky diode is only used for a short time during takeover from N-type power MOSFET and P-type power MOSFET and vice versa. Therefore, a medium-power diode such as Philips PRLL5819 is sufficient.

FEEDBACK RESISTORS R1 AND R2

The output voltage is determined by the resistors R1 and R2. The following conditions apply:

- Use 1% accurate SMD type resistors only. In case larger body resistors are used, the capacitance on ball B2 (feedback input) will be too large, causing inaccurate operation.
- Resistors R1 and R2 should have a maximum value of 57 kΩ when connected in parallel. A higher value will result in inaccurate operation.

Under these conditions, the output voltage can be calculated by the formula: $V_O = 1.24 \times \left(1 + \frac{R1}{R2}\right)$

CURRENT LIMITING RESISTORS

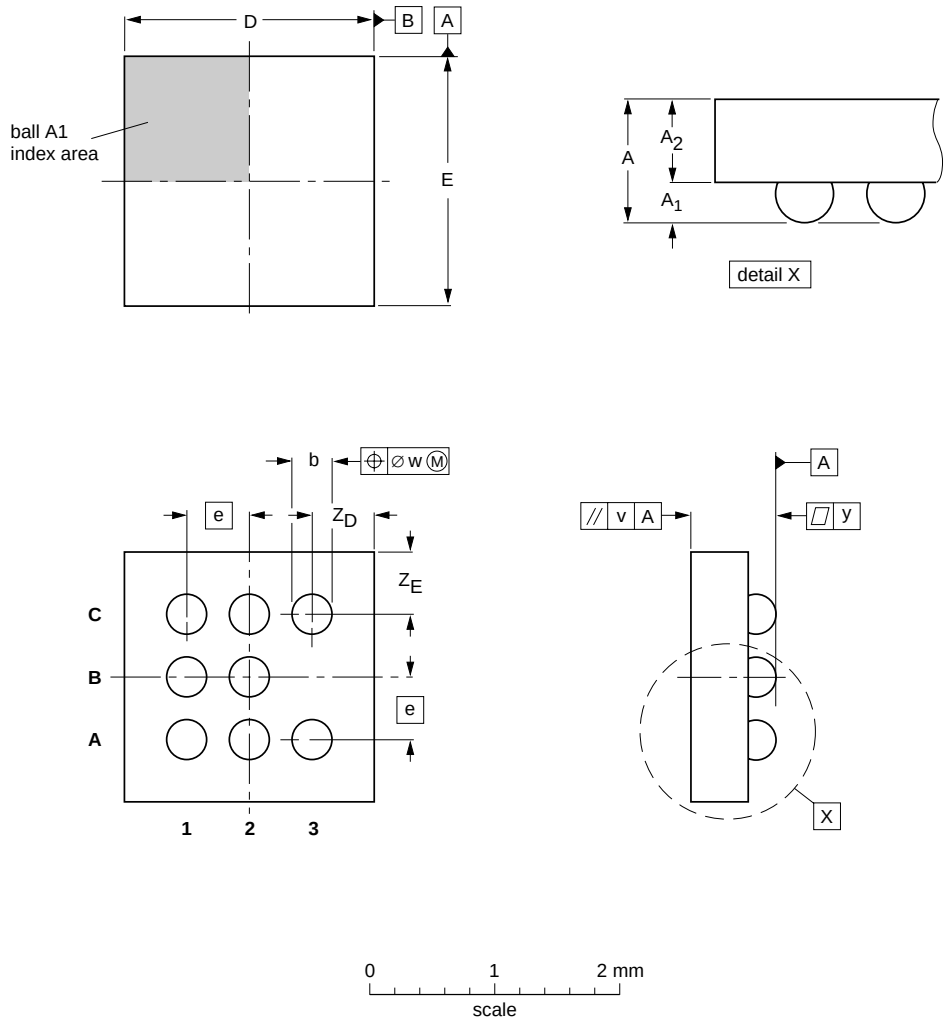
The maximum instantaneous current is set by the external resistors R_{lim}. The preferred type is SMD, 1% accurate. The connection of resistor R_{lim} differs per mode:

- At upconversion (up mode): resistor R_{lim} must be connected between ball C1 (ILIM) and ball A1 (UPOUT/DNIN). The current limiting level is defined by: $I_{lim} = \frac{238}{R_{lim}}$
- At downconversion (down mode): resistor R_{lim} must be connected between ball C1 (ILIM) and ball A3 (GND). The current limiting level is defined by: $I_{lim} = \frac{270}{R_{lim}}$

The average inductor current during limited current operation also depends on the inductance value, input voltage, output voltage and resistive losses in all components in the power path. Ensure that $I_{lim} < I_{sat}$ saturation current of the inductor.

PACKAGE OUTLINE

LFBGA8: plastic low profile fine-pitch ball grid array package; 8 balls; body 2.0 x 2.0 x 0.46 mm TEA1207



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	v	w	y	Z_D	Z_E
mm	0.70	0.28 0.20	0.48 0.44	0.38 0.26	2.05 1.95	2.05 1.95	0.5	0.05	0.1	0.03	0.63 0.38	0.63 0.38

MSD746

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TEA1207						

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective specification	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary specification	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product specification	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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